Roll No. | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 18

B.Tech. (EE) PT (Sem.–3)

DIGITAL ELECTRONICS

Subject Code : BTEE-404

M.Code : 72164

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Answer briefly :

1. How a negative number is accounted in digital system?
2. Draw a foil subtractor using NAND Gate.
3. Draw the logic circuit for the expression $\overline{A}B + A\overline{B}\overline{C}$
4. Write down the applications of D flip flop.
5. Compare ECL and TTL circuits.
6. Draw the logic diagram for the logic function Z = (A+B).C
7. Write down the characteristic table of D Flip-flop.
8. List the differences between decoder and multiplexer.
9. What do you understand from the term digital counter? How it differs from register?
10. What is programmable logic array? How it differs from ROM?

SECTION-B

11. Simplify the Boolean function F(w, x, y, z) = Σ (1, 3, 7, 11, 15), which has the don't-care conditions d(w, x, y, z) = Σ (0, 2, 5).

12. Discuss the working of a 4-bit Johnson counter. Also convert SR into JK and D flipflop.

13. Define the terms resolution and accuracy in context of A/D converter. Also explain the working of parallel A/D converter.

14. What do you understand by the term programmable logic arrays? Classify and explain different types of memories.

15. Design a 3-bit synchronous down counter using j-k flip flops.

SECTION-C

16. Discuss methods of data representations in VHDL. Also explain decision-controlled structure.

17. Design an ECL NOR gate and explain its operation in details. Also compare the performance of static and dynamic memories in details.

18. Write a short notes on:

    a. Quine McCluskey method

    b. HDL format and syntax